Shallow Junction Doping Requirements

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Goals of this presentation

Point out requirements on junction technology besides shallowness.

Investigate the effect of lateral versus vertical junction depth.

Technology Scaling

Smaller is better -- faster, less area.

Industry practices 3D shrinking.

Just print the gate as short as you can, then scale tox, doping and junctions to reduce short channel effects while maintaining performance.

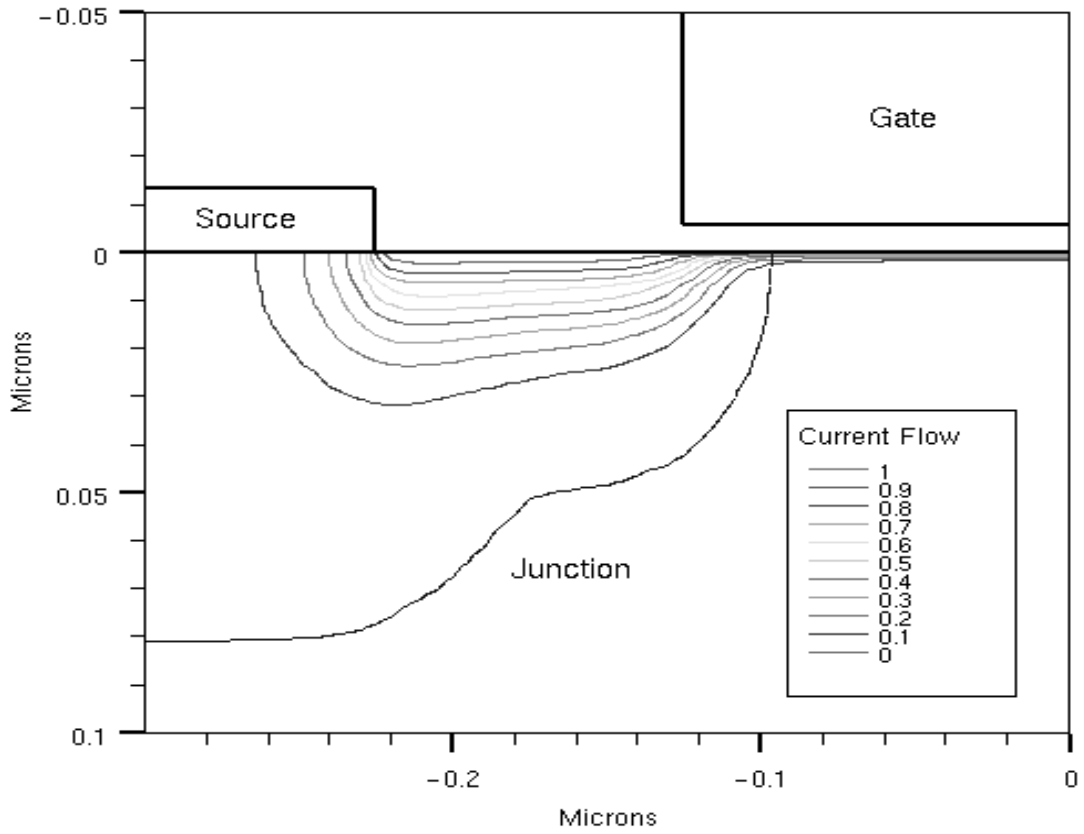
Ioff versus Ion tradeoff.

Shallow, but not too shallow

Shallow junctions are required, but ...

- Need to maintain low sheet resistance.
- Need low contact resistance.
- Need to be deep enough for silicidation.
  - *Silicon consumption and diode leakage.*
- Hence, “deep” S/D and shallow S/D extension.

Current Flow in a MOSFET



Cobalt versus Titanium Silicide

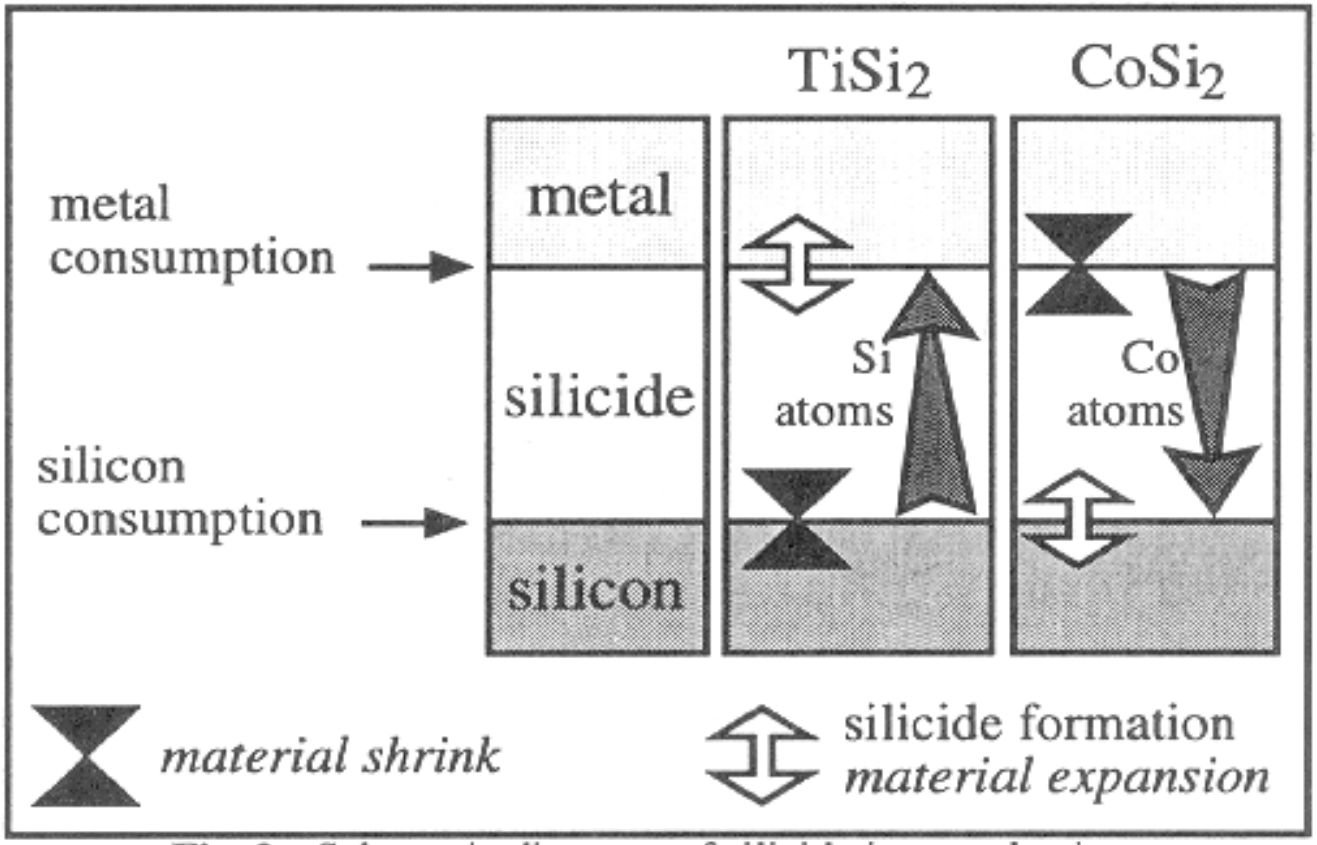


Fig. 2: Schematic diagram of silicidation mechanisms

Fornara and Poncet, CNET, 1996 IEDM, page 73

Impact of Junction Processing on Other Areas

Implantation introduces defects that increase dopant diffusion (TED, RSCE).

Desirable to simultaneously dope the poly gate.

Want high dopant concentration at poly/oxide interface *and* no significant dopant penetration through oxide.

No poly depletion nor boron penetration.

Junction Requirements

Low diffusion resistance beneath silicide
Low contact resistance
Shallow S/D extension
Silicide compatible
Diode leakage much lower than Ioff
Minimal impact on channel profile (RSCE)
Poly gate compatible
Low cost
Uniformity across large wafer
Clean (low particles)
Reliable transistors and contacts
Environment, Safety and Health (ESH)

Part II: Vertical versus Horizontal Junction

Many scaling equations and the NTRS specify a junction depth, without highlighting the 2D nature of junctions.

Horizontal junction “depth” is typically assumed to be 60 to 80% of the vertical depth.

Reasonable assumption for pre-VLSI.

The lateral extent of the junction is more important the vertical depth (shortens channel, increases overlap capacitance).

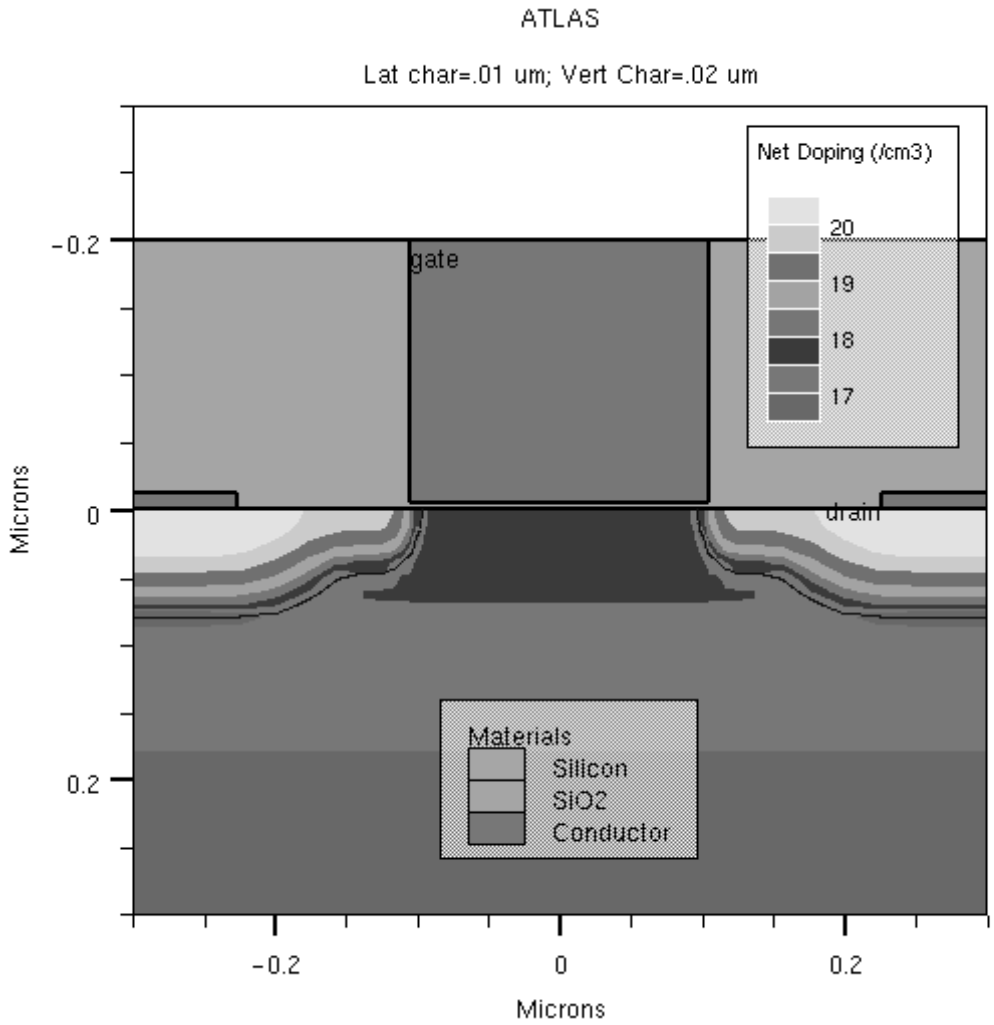
Simulation of Idealized Devices

Transistors were created in a device simulator (PISCES) where the x and y component of the junction was varied independently.

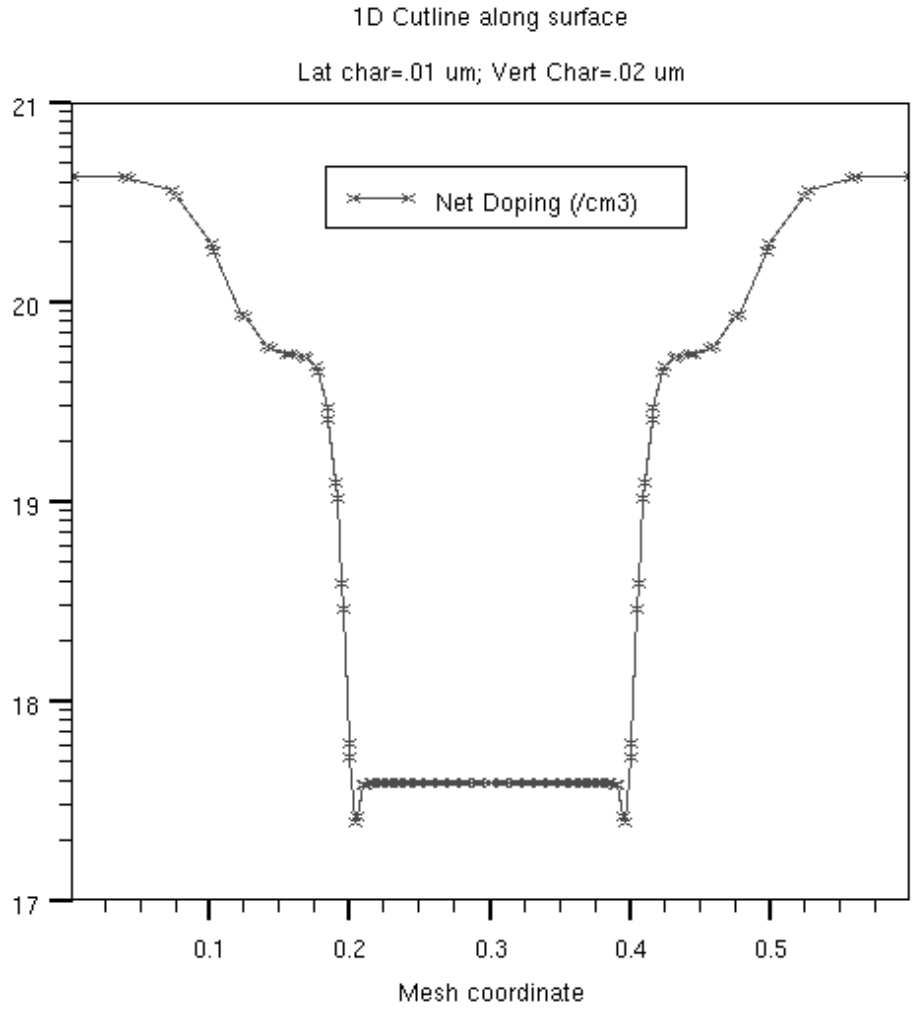
Doping profiles were Gaussian, with a characteristic decay length (one sigma) between 0.01 and 0.04 um.

LDD (S/D extension) doping concentration and the channel length were also varied.

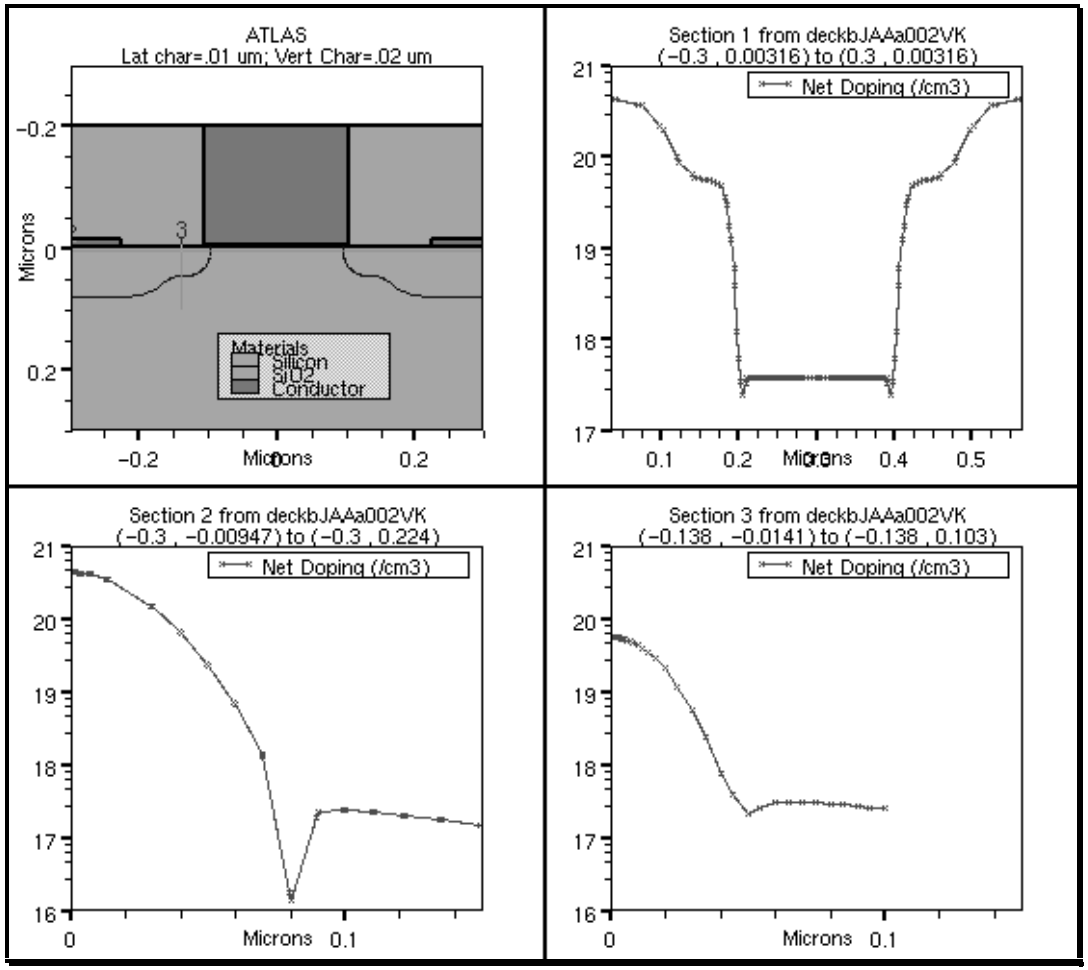
Example Structure



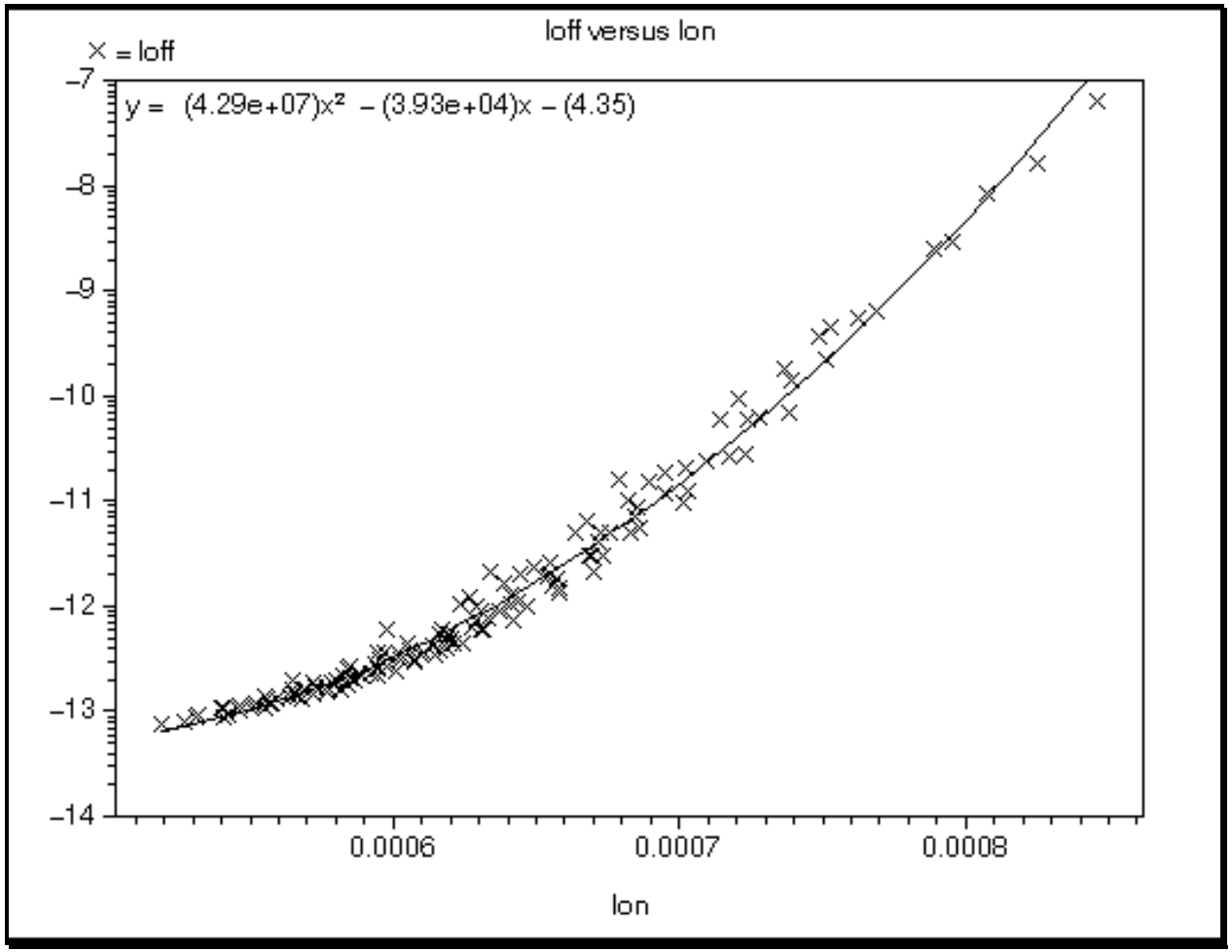
1D Cutline near Surface



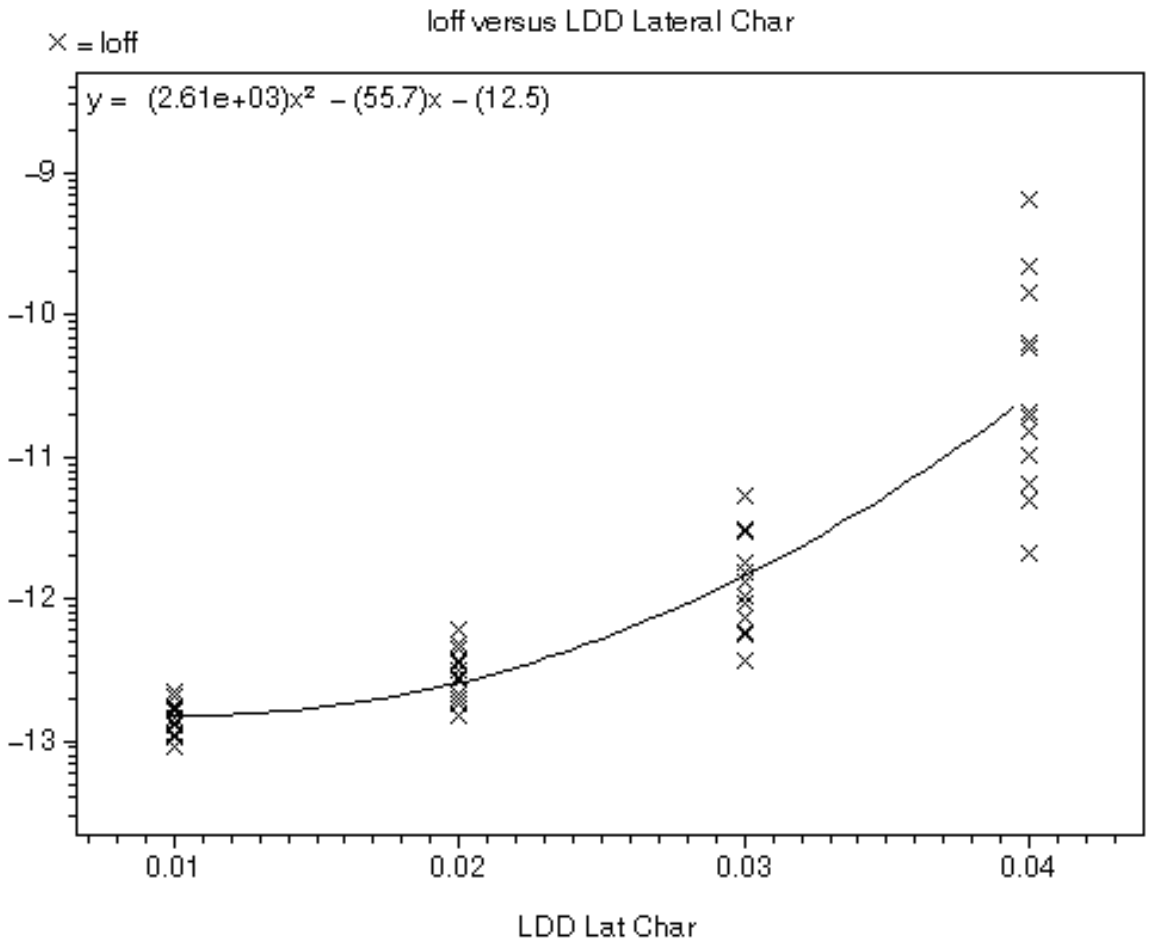
Structure with doping cutlines



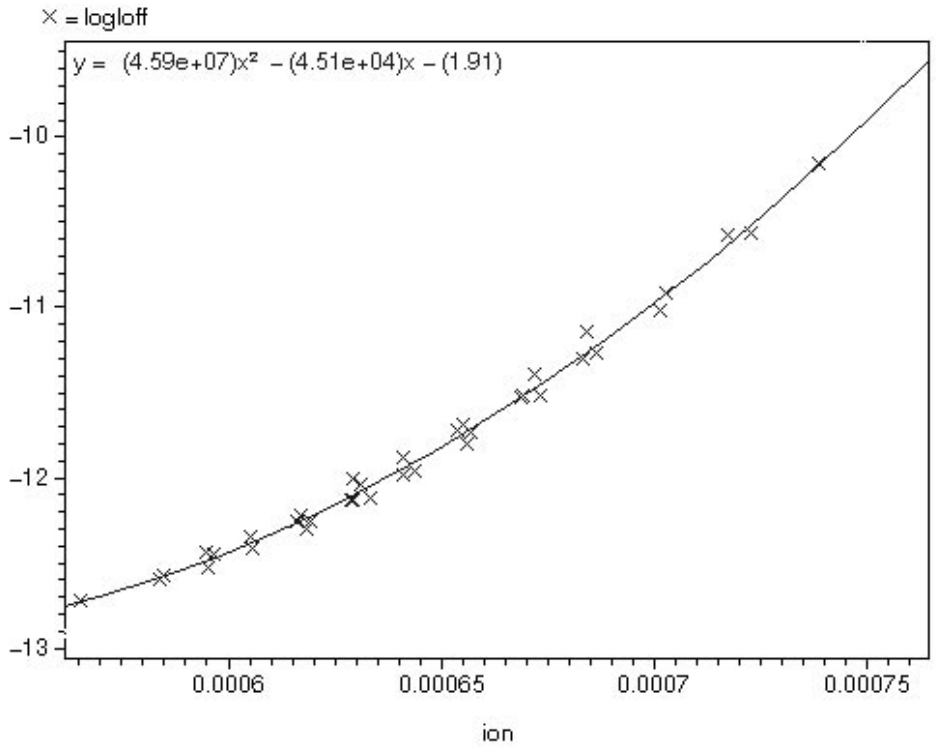
Ioff versus Ion



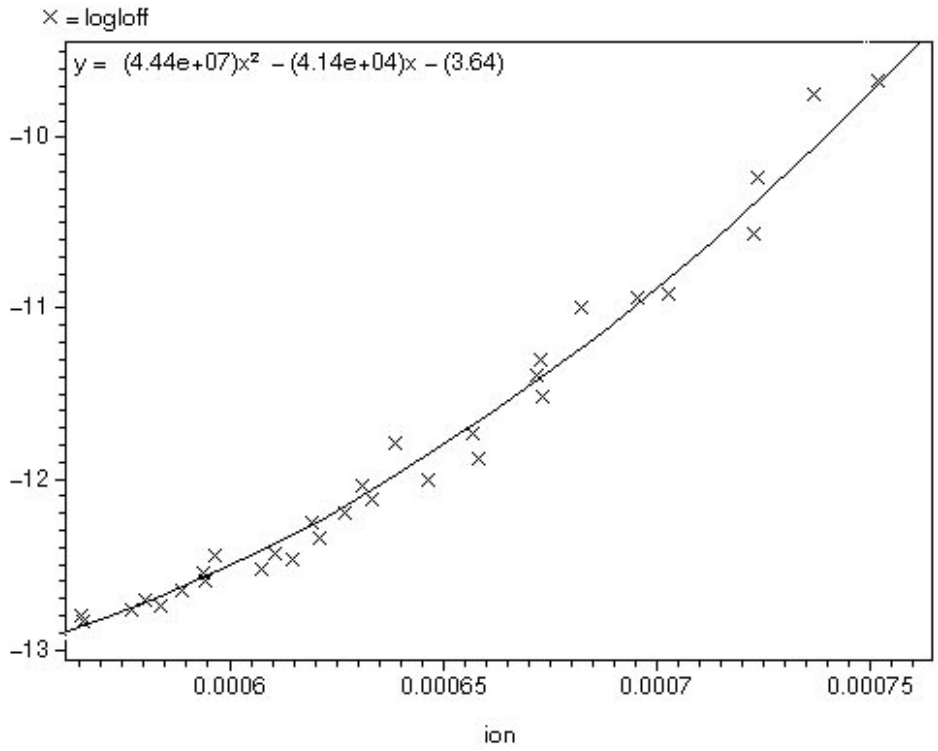
Ioff versus LDD Lateral Characteristic



Ioff for Fixed LDD Lateral Characteristic



Ioff for Fixed LDD Vertical Characteristic



Megahertz

CPU power requirements set Ioff limit.

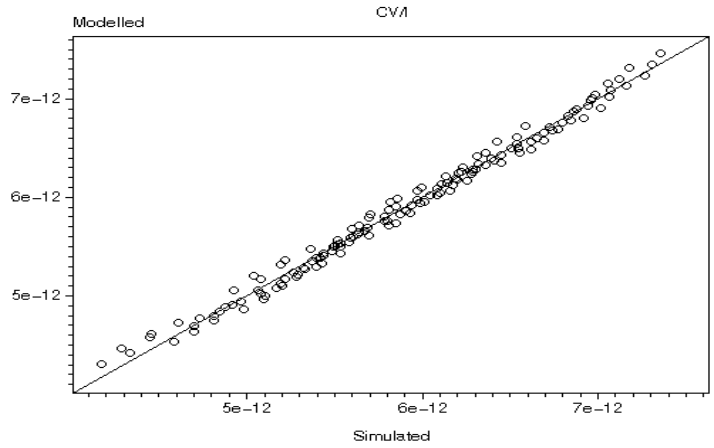
Small changes in Ion (at a given Ioff) are significant.

For a fixed vertical characteristic (.03 um), decreasing the lateral characteristic from .04 to .02 um gives a 4% improvement in Ion.

This translates into a lateral junction difference of .04 um; therefore, junction location control should be much better than this.

Transistor Delay (CV/I)

CV/I = 37.1(L) - .0378(LDD Dose/1e15) - 15.3(LDD Vert Char) - 32.8(LDD Lat Char) - 1.17



Delay is twice as sensitive to changes in lateral char versus vertical char.

Summary

There are many requirements on junction technology besides shallowness - basically, it must integrate into a complete CMOS flow.

Lateral junction control was shown to be more important than vertical junction control.