Re-Examination of 2D Dopant Profiling Needs

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The National Technology Roadmap for Semiconductors (NTRS) has established some stringent requirements on two-dimensional dopant profiling. This work explores the reasons behind these metrology requirements, and also presents the difficulty of achieving these goals from the metrologist's point of view. The goal of this paper is to present a more complete description of the metrology needs, including such issues as dopant statistics, surface profiling, active versus total concentrations, and physical regions of interest in a transistor in order to establish better metrology targets.

INTRODUCTION

Two-Dimensional (2D) dopant profiling has been a highly ranked need in both the process integration and TCAD (simulation) sections of National Technology Roadmap for Semiconductors (NTRS) since its inception. Although some progress has been made in addressing these needs, we are still far from the goals, and the targets continue to shrink. This lack of dopant metrology has *not* affected the rate of technology development. In light of this, the rationale behind the targets is re-examined so that compromises between the desired metrology and what is likely to be achieved can be explored.

METROLOGY TARGETS

The 1997 Roadmap lists the dopant spatial resolution requirements as 5 nm for 250 nm technology and 1 nm for the 70 nm generation (1). The entire row in the table is colored red, meaning *no known solutions*. For most generations, this target is about 1.5% of the transistor gate length (Lgate). This is a reasonable target considering the desired Lgate control of 3-sigma of <10% (2). This equates to 10% control in drain current. This 10% 3-sigma target implies 1-sigma control of roughly 3% in Lgate. Since a MOSFET is a symmetrical device, any movement in the lateral junction location is magnified by a factor of two when determining the source to drain spacing. This distance is often referred to as the effective channel length, Leff, although the electrical channel length is not rigorously the same as the source to drain spacing. Comparing the two targets, we see that the desired resolution in the source to drain spacing (i.e., twice the lateral junction resolution) is approximately the same as the 1-sigma requirement on Lgate control. These targets were set by independent groups, but this comparison shows they are reasonably consistent. A simple statement of the need is that Leff is the most important MOSFET parameter, that we want to control this value to <10%, and therefore would like metrology that is significantly less than 10% of Leff.

The dopant *concentration* precision starts off at 5% for current technology and decreases to 2% at 70 nm (1). A footnote mentions the need for accurate reference materials (standards).

ANATOMY OF A JUNCTION

But what do these targets imply when we start considering the physical characteristics of a modern junction? The dopant concentration near the junction is approximately 1e18/cm^3. A simple estimate of the average dopant spacing can be obtained from the reciprocal of the cube-root of the concentration, or 10 nm in this example. Thus, *the desired spatial resolution near the junction is already lower than the average dopant spacing!* There are two explanations for this paradox. One is the fact that the variation in carrier concentration (electrons or holes) is theoretically smoother than the dopant concentration (3). The carrier profile is more important to the device behavior, although the current metrology requirement is for the dopant profile. This distinction will be discussed more later. The second reason is that we typically perform electrical measurements on structures that are relatively wide, thereby averaging out the variations in source to drain spacing across the width of the structure. This latter point is underappreciated. Rather than the textbook picture of smooth dopant profiles with abrupt junctions, we are entering a regime where we need to consider the location of individual atoms, and how their random location and concentration affects devices (4-7).

For higher concentrations, the situation is improved, although the average dopant spacing only decreases by a factor of 2.2 as the concentration increases by 10x (e.g., at 1E19 atoms/cm^3, the average dopant spacing is 4.6 nm, and decreases further to 2.2 nm at 1e20 atoms/cm^3). The process technologist can gain a better understanding of the dopant metrologist's dilemma by converting the familiar units of atoms/cm^3 to atoms/um^3 or even atoms/nm^3: 1e18 atoms/cm^3 = 1e6 atoms/um^3 = 1e-3 atoms/nm^3. A cube that is 10 nm per side only has one dopant atom in it at

1e18 atoms/cm^3. *Resolution finer than this requires measuring fractions of an atom.* There is an inherent tradeoff between concentration and resolution which is not reflected in the roadmap. There is some irony in the fact that the doping concentrations are lowest (and therefore the hardest to measure) in the regions of most interest. Similarly, changes made in some measurement methods in order to increase the lateral resolution also decrease the measurement sensitivity. For example, 10 nm SIMS spot size results in minute beam currents. Compounding this, the beam energies must be high, which affects the depth resolution (8).

What happens when we consider doping gradients? Assume a 100 nm junction depth, and the concentration dropping by 3 orders of magnitude in that distance. This is a somewhat conservative estimate, in that actual concentration drop will occur over a distance less than the junction depth. The concentration is changing by a decade every 30 nm. Near the junction, the dopant concentration is changing significantly over the average dopant spacing, as shown in the figure below.

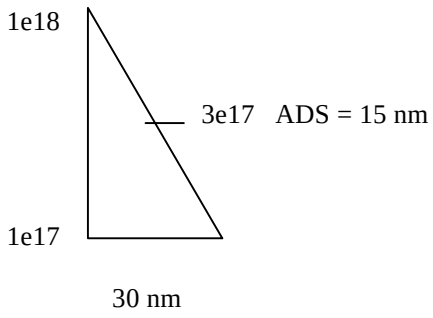

FIGURE 1. Assume the dopant concentration varies by 1 decade every 30 nm. For a background concentration of 3e17 atoms/cm^3, the average dopant spacing (ADS) is 15 nm. Thus, *near the junction, the dopant concentration is changing by 3x over the ADS.*

This example leads to a second paradox. A 1D SIMS profile of the S/D dopant will show a smooth and continuous transition between 1e18 and 1e17 atoms/cm^3. But at a local level, the average dopant spacing at 1e18 atoms/cm^3 is 10 nm, and 22 nm at 1e17 atoms/cm^3. The sum of these two distances is equal to the 30 nm in the figure above. That is, we imagine the dopant as varying smoothly from 1e18 to 1e17 atoms/cm^3, yet a simple calculation of the average dopant spacing in this example shows there is no room over this distance to "fit in" the intermediate concentrations (2e17, 3e17, 4e17, etc.). A smooth and continuous profile only occurs when we average over a large area, yet a transistor operates at a very local level.

Current devices may already be running into some of these statistical limits. Consider again the average dopant spacing of 10 nm near the junction. The minimum transistor width is often twice the minimum length. For 250 nm technology, this would mean that there would only be 50 dopant atoms along the width of the device near the junction. Several researchers have investigated the fluctuations that will result from the random variation in the number of dopant atoms, although these have been primarily focused on dopants in the channel and how that affects threshold voltage. The source to drain spacing is a key parameter in controlling the transistor, and the stochastic nature of this spacing may turn out to be a more important factor and hit us sooner than the random dopant variation in the channel.

The roadmap alludes to the need for 3D profiling as well, but it should be remembered that current 2D methods are already quasi-3D, in that they probe into the silicon a small, finite depth (10's of nm, depending on the concentration and technique). Most 2D methods require elaborate sample preparation, and it is difficult to imagine extending these techniques to 3D. An alternative approach may be to measure 2D profiles on two or more sides of a box, and to infer the 3D profile. More specifically, the conventional 2D cross-section coupled with a "top-down" view of the device might provide much of the desired information (9). In the top-down view, the poly gate would be removed, and local variations in the source to drain spacings would be measured.

Dopant statistics also has interesting implications for device simulation. Most simulations today are 2D, with a simulation grid that is finer than the average dopant spacing. Again, this is related to assumptions of carriers profiles varying more rapidly than dopant profiles, and of implicit averaging over wide structures. For 3D simulations, especially those statistical in nature, careful attention should be paid between the simulation grid and the average dopant spacing (10).

NEEDS AND REQUIREMENTS

This section will consider further what the dopant metrology needs are, particularly from a motivational viewpoint, and will also discuss important needs that are *not* in the current roadmap. The need for 2D profiling has been present for a long time, and is not new to deep sub-micron technologies. Indeed, it should be asked whether the need is any greater now than before. It is possible that the need was greatest at the time lightly doped drain (LDD) structures were introduced. Power supply voltages were still at 5 volts, and the resulting electric fields were so high that the transition region from high to low doping (i.e., the junction) had to be intentionally widened, which degraded the transistor performance (one of the key reliability-versus-performance tradeoffs the industry has faced). Since that time, supply voltages have better

scaled with the channel length, and the "LDD" concentration has steadily increased to the point where it is more accurate to refer to this region between the channel and the deep source/drain (S/D) as the "S/D extension". Although this remains a key region for defining transistor behavior, the dynamic range (Max - min concentration) has decreased substantially, and hot-electrons are less and less of a problem as the supply voltage continues to shrink. This has reduced somewhat the interest in detailed lateral profiling in this region of the transistor.

Implicit in the roadmap is profiling of the S/D. But other regions of the transistor have increased in importance. The reverse short channel effect (RSCE) is the unexpected maximum in threshold voltage as channel length is reduced (11). Damage from the S/D implant migrates to the channel region where it causes a pile-up of channel dopant at the surface. Although we have a reasonable understanding of this effect, this has increased the need for 2D profiling *in the channel*, where doping concentrations are lower than in the S/D extension (mid-1e17 atoms/cm^3 to low-1e18 atoms/cm^3). Because this effect is channel-length dependent, the need for profiling is on actual transistors, not large area test structures. Profiling of point-defects (vacancies and interstitials) in this region is almost as important as dopant profiling.

More recently, large amounts of "dose loss" have been observed at the silicon/oxide interface (12-13). It is not uncommon for 50% of a shallow implant to be trapped and electrically inactive at this interface. Note that this is primarily a 1D metrology problem. This effect creates a need for improved profiling near the silicon surface.

Dose loss leads into the issue of the different "types" of profiles. Although these definitions can be found in many textbooks, they are worth reviewing here. First, there is the difference between electrically active and the total concentration. Under the electrically active category, there is electrically active dopant versus electrically active carrier concentration. There is also the need to distinguish between the "net" concentration (donors - acceptors, or electrons - holes) versus individual dopant species. Different techniques measure different profiles. In many cases, the different types of profiles are similar. But it is important to distinguish which type of profile is being measured. It is the electrically active, net carrier profile that directly relates to device behavior. Of course, the carrier profiles are bias dependent (gate, source, drain and substrate biases). Techniques which allow biases to be applied to the device can be very instructional. However, there is not a strong need for this capability, as it is assumed that the carrier profiles can be determined from knowledge of the dopant profiles via a device simulator. For issues such as dose loss, it is important to be able to measure both the total and active concentrations. This may require two different measurement techniques.

A similar profiling problem arises at the silicon/silicide interface. It is important to have high dopant concentration at this interface to reduce contact resistance. During silicide growth, the dopants could segregate into the silicide. To date, dopant loss at this interface has not been reported as a significant problem, but it is mentioned here in case there are any special metrology issues arising from presence of a silicide. This interface is typically not very smooth, which leads to local variation in the distance between the silicide and the S/D junction. If this distance becomes too shallow, the diode leakage current can increase.

Another region of increased importance is in the poly gate. Historically, this region was considered to be a metal because it was so heavily doped. But as oxides get thinner, dopant penetration from the poly gate through the gate oxide becomes more of a problem, so the dopant concentration is reduced to help prevent this. This can lead to a side-effect known as "poly-depletion," whereby a small depletion layer forms at the poly/oxide interface under high gate bias. Poly-depletion is exacerbated by thinner gate oxides, and also contributes a more substantial fraction to the total effective gate capacitance as the oxide thickness is reduced. Technologists are trying the balance the tradeoffs between poly-depletion and dopant penetration (too little versus too much dopant at the poly/gate-oxide interface). The process technologist is interested in knowing the electrically active concentration at the bottom of the poly (tens of nm from the gate oxide). They are also interested in knowing whether any poly dopant penetrates through the gate oxide and into the channel, although electrical techniques (i.e., threshold voltage shifts) can satisfy this requirement. Actually, CV measurements can do a reasonable job of estimating the dopant concentration at the poly/oxide interface as well, although occasional direct measurement would be desirable.

We now return to the motivation for these stringent dopant profile requirements. This is largely driven by the need for "predictive" TCAD. Ideally, you would like to be able to accurately simulate a technology before you build it. However, there is great value in approximate results (14), which require less accuracy. Given the rapid pace of technology development, it is difficult, if not impossible, to achieve predictive TCAD. Although predictive TCAD remains a desirable goal, it may not be a realistic one, and it is this goal that imposes the strict dopant profiling requirements. We can also examine the dopant profiling needs from the other direction: given the current state of 2D profiling, *any* information is useful. As an example, simply determining the junction location may be as useful as the more complete dopant profile, and

some measurement techniques are well suited for establishing junction locations (15-16). It is the lateral junction location *near the surface* that is of most interest. If one could correctly predict this lateral junction location and the 1D vertical S/D profile, you could have reasonable confidence in your ability to predict the whole profile (17). As an interesting sidenote, *perfect* dopant metrology would not necessary result in predictive TCAD. Knowing the final dopant profile is not enough to guarantee that you could build a model to predict the results.

The source to drain spacing, or the lateral junction location, has been mentioned as a key requirement. It can be just as important to know this location *with respect to* the gate edge. The source to drain spacing controls the DC, or steady-state characteristics of a device. But the transient, or switching, characteristics of a device are heavily influenced by the amount of capacitance between the gate and the source/drain. The distance that the S/D diffuses under the gate controls this overlap capacitance. These dopant profiling requirements are summarized in the following table.

TABLE 1. Dopant Profiling Needs

Lateral junction location at silicon *surface*.
Distance from surface junction to gate edge (overlap).
2D *channel* profiles (top-down measurement?).
2D *point-defect* profiles.
1D surface profiling (dose loss).
1D active concentration at bottom of poly.

Rank ordered list of dopant profiling needs. In general, a distinction is not made between carrier or dopant profiles, under the assumption that dopant profiles can be converted to carrier profiles in a device simulator (the reverse process is not as straightforward).

ELECTRICAL ALTERNATIVES

It would be remiss to not mention the increased activity in inverse modeling to determine dopant profiles (18-19). In this approach, dopant profiles are inferred via iteration of electrical measurements and device simulation. Perhaps the greatest advantage to this technique is the possibility of obtaining across-the-wafer variations. Most direct measurement techniques are too time-consuming to accomplish this. Inverse modeling is well suited to the extraction of 2D profiles. When combined with conventional 1D profiling techniques, inverse modeling could possibly satisfy most process integration and modeling needs.

SUMMARY

This paper has intended to build a bridge between process technologists and dopant metrology experts by more clearly stating the dopant profiling needs. Continued discussions between the two groups should lead to better compromises between what is desired and what is achievable. The current Roadmap goals are very aggressive, but that shouldn't imply that less aggressive results would not still be useful to technologists. TCAD and dopant metrology are not technology showstoppers, but small improvements in our predictive and diagnostic capabilities can have high payback.

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